03-06-06
10,611,396
COFC

Docket No.: 08211/0200242-US0
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Wai Cheong Chan et al.

Patent No.: 6,965,264

Issued: November 15, 2005

For: ADAPTIVE THRESHOLD SCALING

REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.322

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted several Patent Office errors which should be corrected.

In the Title:

Please delete "ADAPTIVE THRESHOLD SCALING CIRCUIT" and substitute

-- ADAPTIVE THRESHOLD SCALING --.

In the claims:

Column 6, Line 7, In Claim 10, after "transistors" insert --,--.

Column 6, Line 23, In Claim 12, delete "claim 11", and insert -- claim 10,--.

The erros were not in the application as filed by applicant; accordingly no fee is required. Enclosed please find marked up copies of the Issue Fee transmittal and the Amendment in reponse to Non-Final Office Action filed on March 10, 2005.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

Dated: March 2, 2006

Respectfully submitted,

By _____

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Attorneys/Agents For Applicant

Application Number (if known): 10/611,396 Attorney Docket No.: 08211/0200242-US0

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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.	:	6,965,264
APPLICATION NO.	:	10/611,396
ISSUE DATE	:	November 15, 2005
INVENTOR(S)	:	Wai Cheong Chan et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Title:

Please delete "ADAPTIVE THRESHOLD SCALING CIRCUIT" and substitute

-- ADAPTIVE THRESHOLD SCALING --.

In the claims:

Column 6, Line 7, In Claim 10, after "transistors" insert --,--.

Column 6, Line 23, In Claim 12, delete "claim 11", and insert -- claim 10,--.

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
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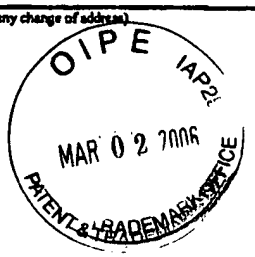

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,396	06/30/2003	Wai Cheong Chan	~~08211/0200242-US0~~	6850

TITLE OF INVENTION: ~~ADAPTIVE THRESHOLD SCALING CIRCUIT~~

08211/0200242-US0/P05556

ADAPTIVE THRESHOLD SCALING

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$0	$1400	07/27/2005

EXAMINER	ART UNIT	CLASS-SUBCLASS
CUNNINGHAM, TERRY D	2816	327-537000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Darby & Darby PC
2 John W. Branch
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: National Semiconductor Corporation

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Santa Clara, California

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:
- ☑ Issue Fee
- ☐ *Publication Fee (No small entity discount permitted)*
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):
- ☑ A check in the amount of the fee(s) is enclosed.
- ☐ *Payment by credit card. Form PTO-2038 is attached.*
- ☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above. NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date June 8, 2005

Typed or printed name John W. Branch Registration No. 41,633

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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0 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Wai C. Chan et al.

Application No.: 10/611,396 Confirmation No.: 6850

Filed: June 30, 2003 Art Unit: 2816

For: ADAPTIVE THRESHOLD SCALING Examiner: T. D. Cunningham

AMENDMENT IN RESPONSE TO NON-FINAL OFFICE ACTION

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated December 10, 2004 (Paper No. 12072004), please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An apparatus for reducing a leakage current for a plurality of MOS transistors disposed in an integrated circuit, comprising:

a detection circuit for automatically generating an up signal and a down signal based on a determination as to what side of an inflection point that an initial value of the leakage current is disposed, wherein the inflection point is a graphical representation of a value for a back bias voltage that causes the least amount of leakage current from the plurality of MOS transistors, and wherein the detection circuit further includes at least two current mirrors that are arranged with complementary MOS transistors that have a relatively matched size; and

a bias circuit for automatically providing an adjusted back bias voltage that enables the least amount of leakage current by the plurality of MOS transistors, wherein if the up signal is generated, then the adjusted back bias voltage is increased and if the down signal is generated, then the adjusted back bias voltage is decreased, and wherein the biasing circuit provides a relatively constant value for the back bias voltage if both the up signal and the down signal are ungenerated by the detection circuit.

2. (Original) The apparatus of Claim 1, wherein the plurality of MOS transistors are PMOS transistors, wherein if the initial leakage current is disposed before the inflection point, the up signal is generated and the adjusted back bias voltage is increased, and wherein if the initial leakage current is disposed after the inflection point, the down signal is generated and the adjusted back bias voltage is decreased.

3. (Original) The apparatus of Claim 1, wherein the plurality of MOS transistors are NMOS transistors.

4. (Original) The apparatus of Claim 1, wherein the detection circuit further includes a logic circuit that activates the biasing circuit with up and down signals that are based on a comparison of at least three voltages generated by at least three leakage currents in at least two pairs

of MOS transistors of a relatively matched size, wherein the matched pairs of MOS transistors are coupled to separate current mirrors that are arranged with complementary MOS transistors that have a relatively matched size.

5. (Original) The apparatus of Claim 1, wherein the detection circuit further includes a logic circuit that employs at least three voltages to band the position of the inflection point, wherein the at least three voltages are generated by at least three leakage currents in at least two pairs of MOS transistors of a relatively matched size, wherein the matched pairs of MOS transistors are coupled to separate current mirrors that are arranged with complementary MOS transistors that have a relatively matched size.

6. (Original) The apparatus of Claim 1, wherein the detection circuit further includes at least two pairs of MOS transistors of a relatively matched size, wherein the matched pairs of the MOS transistors are sized substantially larger than a minimum size for the plurality of MOS transistors, and wherein the substantially larger size of the matched MOS transistors enables the initial leakage current to be detectable by the detection circuit.

7. (Cancelled)

8. (Original) The apparatus of Claim 1, wherein the back bias voltage is coupled to a substrate shared by the bulk terminals for the plurality of MOS transistors.

9. (Original) The apparatus of Claim 1, wherein the back bias voltage is a reverse bias voltage applied to a bulk terminal of the plurality of MOS transistors.

10. (Original) The apparatus of Claim 1, further comprising a battery that supplies power to the integrated circuit, wherein the reduction in the value of the leakage current causes a decrease in the amount of power drawn in an idle state by the integrated circuit from the battery.

11. (Currently Amended) An integrated circuit that reduces a leakage current for a plurality of PMOS transistors disposed in an integrated circuit, comprising:

a detection circuit for automatically determining on what side of an inflection point that an initial value of the leakage current is disposed, wherein the inflection point is graphical representation of a value for a back bias voltage that causes a least amount of leakage current from the plurality of PMOS transistors, wherein if the initial value of the leakage current is disposed before the inflection point, an up signal is generated, and wherein if the initial leakage current is disposed after the inflection point, a down signal is generated; and wherein the PMOS transistors in the detection circuit are of a relatively matched size that is substantially larger than a minimum size for the plurality of PMOS transistors, and wherein the substantially larger and matched size of the PMOS transistors in the detection circuit enables the initial leakage current to be detectable by the detection circuit; and

a bias circuit for automatically providing a back bias voltage that enables the least amount of leakage current by the plurality of PMOS transistors, wherein if an up signal is generated, then the magnitude of the back bias voltage is increased and if a down signal is generated, then the magnitude of the back bias voltage is decreased, and wherein the biasing circuit provides a relatively constant value for the back bias voltage if both the up signal and the down signal are ungenerated by the detection circuit.

12. (Original) The integrated circuit of Claim 11, wherein the integrated circuit is fabricated with a sub-micron process.

13. (Original) The integrated circuit of Claim 11, wherein the detection circuit further includes a logic circuit that activates the biasing circuit with up and down signals that are based on a comparison of at least three voltages that are adjusted to band the position of the inflection point, wherein the middle voltage is selected for the adjusted back bias voltage.

14. (Cancelled)

15. (Original) The integrated circuit of Claim 11, wherein the back bias voltage is a reverse bias voltage that is applied to a bulk terminal of the plurality of PMOS transistors.

16. (Currently Amended) An integrated circuit that reduces a leakage current for a plurality of NMOS transistors disposed in an integrated circuit, comprising:

a detection circuit for automatically determining on what side of an inflection point that an initial value of the leakage current is disposed, wherein the inflection point is graphical representation of a value for a back bias voltage that causes a least amount of leakage current from the plurality of NMOS transistors, wherein if the initial value of the leakage current is disposed before the inflection point, an up signal is generated, and wherein if the initial leakage current is disposed after the inflection point, a down signal is generated, and wherein the NMOS transistors in the detection circuit are of a relatively matched size that is substantially larger than a minimum size for the plurality of NMOS transistors, and wherein the substantially larger and matched size of the NMOS transistors in the detection circuit enables the initial leakage current to be detectable by the detection circuit; and

a bias circuit for automatically providing a back bias voltage that enables the least amount of leakage current by the plurality of NMOS transistors, wherein if an up signal is generated, then the magnitude of the back bias voltage is decreased and if a down signal is generated, then the magnitude of the back bias voltage is increased, and wherein the biasing circuit provides a relatively constant value for the back bias voltage if both the up signal and the down signal are ungenerated by the detection circuit.

17. (Cancelled)

REMARKS

Claims 1-17 are pending in the Office Action dated December 10, 2004. Claims 1-3, 8-13 and 15-17 were rejected. Also, Claims 4-7 and 14 were objected to. Claims 1, 11 and 16 have been amended. Claims 7, 14, and 17 have been cancelled.

Objected To Claims

The present Office Action has objected to Claims 4-7 and 14 as being dependent on a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In response to the present Office Action, independent Claim 1 has been amended to include substantially the same subject matter of dependent Claim 7. Also, independent Claims 11 and 16 were amended to include substantially the same subject matter of dependent Claim 14. Therefore, amended independent Claims 1, 11, and 16 are now in condition for allowance. Additionally, Claims 2-6, 8-10, 12, 13, and 15 are now allowable at least for the same reasons as the amended independent claims upon which they depend.

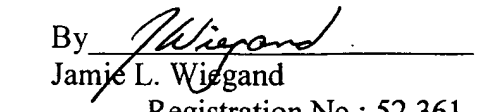
35 USC § 102 Rejections

The Office Action has rejected Claims 1-3, 8-13, and 15-17 under 35 USC § 102(b) as being anticipated by U.S. Patent No. 6,489,833. The Office Action found that the '833 patent disclosed all of the elements of the rejected claims.

Although applicant respectfully disagrees with the Office Action's rejections for several reasons, these rejections are now moot in view of the amendments to the independent claims as discussed above. Additionally, in view of the above amendments, the Examiner is asked to pass this pending application to allowance at the earliest convenience.

Dated: March 10, 2005

Respectfully submitted,

By 

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